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ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/554,143	BOLCATO ET AL.	
	Examiner	Art Unit	
	JASON PROCTOR	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/20/05, 9/29/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-23 are submitted for examination.

Claims 1-23 are rejected.

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on 29 September 2006 and 20 October 2005 were filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Interpretation - 35 USC § 101

2. Claims 1-12 define a method of simulating a circuit using an analog or RF simulator. In the context of the disclosure, this method is interpreted as being inherently tied to a computing device. These claims are therefore found to meet the requirements of 35 U.S.C. § 101 for statutory subject matter.

3. Claims 18-21 define a simulator for simulating a circuit. In the context of the disclosure, this simulator is interpreted as being inherently tied to a computer device. However, these claims recite "means for" limitations that are not adequately described by the disclosure, as explained below. These claims appear to meet the requirements of 35 U.S.C. § 101 for statutory subject matter because these claims appear to define an apparatus.

If Applicants find this interpretation improper or undesirable, clarification or amendment of the claim language is required.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 13-17 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Claim 13 defines "an analog or RF simulator for simulating a circuit" comprising "an elaboration engine" and "a simulation kernel". In the context of the specification, the claimed simulator is computer software per se. Computer software per se is none of the categories of invention set forth in 35 U.S.C. § 101. Claim 13 is therefore directed to non-statutory subject matter. None of dependent claims 14-17 overcome this deficiency.

5. Claims 21-23 are rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

Claims 21-23 define a method for simulating a circuit comprising the steps of "generating a system of equations...," "solving the system of equations...," and "outputting the simulation results." The claim consists entirely of abstract mathematical steps, and is neither inherently nor expressly tied to any particular apparatus. The method does not transform any underlying subject matter to a different state or thing. Therefore, these methods to not define statutory subject matter as required by 35 U.S.C. § 101.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 18-20 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 18-20 recite an apparatus claim having several "means for" limitations. The disclosure of the application does not describe adequate structure to support these limitations. The specification describes a method for performing a simulation, but does not contain any detailed description of a structure or apparatus that implements the same method. Therefore, claims 18-20 which recite "means for" limitations that must be interpreted according to 35 U.S.C. § 112, sixth paragraph, do not find adequate written description support in the application as filed.

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 8 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites mathematical notation without describing what the symbols represent. This claim language is vague and indefinite.

8. Claim 9 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites that "J is a Jacobian matrix related to the circuit components" and also that the "matrix J [is] built using the second circuit description". It is unclear how to interpret these phrases in the same claim. It appears that the claim recites a broad definition for the matrix J followed by a narrower definition for same matrix. The scope of this claim language is vague and indefinite.

Claim 9 recites that "$F(X^i)$ is an evaluated equation" and "evaluating $F(X^i)$ using the first circuit description". It is unclear how to interpret these phrases. The relationship between $F(X^i)$ and the first circuit description is unknown. The claim appears to specify that the first circuit description represents a circuit that can evaluate $F(X^i)$. This does not appear to conform to the disclosed invention. Clarification or correction is required. The scope of this claim language is vague and indefinite.

9. Claim 10 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 is a "use" claim that merely recites applications for which the analog simulation and RF simulation can be used. This language does not further define the method of the parent claims. The scope of this claim is vague and indefinite.

10. Claim 10 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 appears to recite a separate and distinct method from the parent claim 1. None of the elements in claim 10 refer back to claim 1 or relate to the elements of claim 1. Claim 10 does not further limit any of the method steps recited in claim 1. Claim 10, when written in independent form, appears to include two different inventions. The scope of this claim is vague and indefinite.

11. Claim 15 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites the phrase "a DSPF" which is apparently an acronym that is defined by neither the claim nor the specification. The use of this term in the claims should be accompanied by the industry-standard definition for the acronym. In its present state, the claim is vague and indefinite.

12. Claim 16 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites mathematical notation without describing what the symbols represent. This claim language is vague and indefinite.

13. Claims 18-20 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 18-20 recites an apparatus claim with several "means for" limitations. It is unclear what structure disclosed in the specification constitutes the claimed "means for". The Examiner respectfully submits that there does not appear to be sufficient disclosure of structure for performing these functions to support a "means for" limitation in an apparatus claim.

14. Claim 20 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 recites mathematical notation without describing what the symbols represent. This claim language is vague and indefinite.

Additionally, claim 20 attempts to further limit that "means for simulating" element of the "simulator" apparatus, but recites a method step. It is unclear how to interpret this claim

language. This language appears to recite a method step that is intended to further limit a structural limitation. This claim language is vague and indefinite.

Additionally, claim 20 recites "factorizing a matrix J using the second circuit description" which appears to mean that the second circuit description represents a circuit that can factor the matrix J. This does not appear to conform to the disclosed invention. Clarification or correction is required. The scope of this claim language is vague and indefinite.

15. Claim 23 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23 recites "the modified circuit description" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 1-3, 7, and 10 are rejected under 35 U.S.C. § 102(e) as being anticipated by US Patent No. 7,003,753 to Teene.

Regarding claim 1, Teene discloses a method of simulating a circuit using an analog or RF simulator [*"More specifically, but without limitation thereto, the present invention relates to methods of representing an integrated circuit design for simulating the operation of the integrated circuit."* (Teene, column 1, lines 8-12)], comprising:

defining two circuit descriptions to be used during the simulation, a first circuit description used for accuracy of the simulation and a second circuit description, different from the first circuit description, used for increasing the speed of the simulation; and simulating the circuit using both the first and second circuit descriptions [*"The functional simulation of FIG. 4 may include parasitic capacitance but generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation of the integrated circuit design."* (Teene, column 3, lines 60-64); *"In the full instance resistance and capacitance extraction block 502, a layout extraction is performed to determine the values of all the parasitic capacitances and resistances in the integrated circuit design to generate the flat RC netlist for simulating the operation of the integrated circuit."* (Teene, column 4, lines 10-14)].

Regarding claim 2, Teene discloses that the first circuit description comprises parasitic information and the second circuit description has the parasitic information removed or substantially reduced [*"The functional simulation of FIG. 4 may include parasitic capacitance but generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation of the integrated circuit design."* (Teene, column 3, lines 60-64); *"In the full instance resistance and capacitance extraction block 502, a layout extraction is performed to determine the values of all the parasitic capacitances and resistances in the*

integrated circuit design to generate the flat RC netlist for simulating the operation of the integrated circuit." (Teene, column 4, lines 10-14)].

Regarding claim 3, Teene discloses reading a netlist comprising parasitic information or reading a netlist and a separate file containing parasitic information, and wherein the first circuit description comprises all of the elements included in the netlist plus the parasitic information [*"The functional simulation of FIG. 4 may include parasitic capacitance but generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation of the integrated circuit design."* (Teene, column 3, lines 60-64); *"In the full instance resistance and capacitance extraction block 502, a layout extraction is performed to determine the values of all the parasitic capacitances and resistances in the integrated circuit design to generate the flat RC netlist for simulating the operation of the integrated circuit."* (Teene, column 4, lines 10-14)].

Regarding claim 7, Teene discloses a method further comprising:

forming a first list comprising circuit components without parasitic information [*"The functional simulation of FIG. 4 may include parasitic capacitance but generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation of the integrated circuit design."* (Teene, column 3, lines 60-64);

forming a second list comprising the parasitic information [*"Accurate simulation and design analysis of large structured arrays typically produced in sub-micron technologies*

generally require back-annotation of the netlist to include parasitic resistance and capacitance." (Teene, column 3, lines 64-67)];

forming first and second simulation data structures using the first and second lists, respectively [*"FIG. 4 illustrates a flow diagram 400 for simulating a hierarchical integrated circuit design including only capacitance based on a logical netlist according to the prior art."* (Teene, column 3, lines 47-49); *"In the full instance resistance and capacitance extraction block 502, a layout extraction is performed to determine the values of all the parasitic capacitances and resistances in the integrated circuit design to generate the flat RC netlist for simulating the operation of the integrated circuit."* (Teene, column 4, lines 10-14)], and

wherein the first circuit description is defined as a combination of the first and second lists, and the second circuit description is defined as only the first list [(Teene, column 3, lines 47-49); (Teene, column 4, lines 10-14)].

Regarding claim 10, Teene discloses a simulation method that can be used for any desired application. Therefore, Teene discloses that the analog simulation is used for any one or more of the following: DC, AC, and transient analysis and the RF simulation is used for state-state analysis and modulated steady-state analysis.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. § 103(c) and potential 35 U.S.C. § 102(e), (f) or (g) prior art under 35 U.S.C. § 103(a).

17. Claims 4-5 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Teene.

Regarding claim 4, Teene teaches comprising modifying the first circuit description to generate the second circuit description with reduced parasitic information, wherein modifying comprises: analyzing the first circuit to create parasitic information (Teene, column 3, lines 47-49); (Teene, column 4, lines 10-14).

Teene does not expressly teach analyzing values and functionality of electrical components in the circuit to determine which components are parasitic information; and

removing the parasitic information based on the analysis.

Teene also teaches that the method steps may be performed in another order [*"Although the method of the present invention illustrated by the flowchart descriptions above are described and shown with reference to specific steps performed in a specific order, these steps may be combined, sub-divided, or reordered without departing from the scope of the claims."* (Teene, column 7, lines 44-48)].

It would have been obvious to a person of ordinary skill in the art to perform a method that follows Teene's method to produce a second circuit description with parasitic information included, and to remove that parasitic information to return to a previous stage in the method. This could result from a simulation involving the second circuit description including the parasitic information that reveals unacceptable performance or an error in the circuit design. It would then be common sense and common knowledge to a person of ordinary skill in the art to 1) optionally modify the second circuit design to address the problem, remove the parasitic information, and return to a previous step in the design process; or 2) remove the parasitic information, return to a previous step in the design process, and modify the design at a previous step to address the problem.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to follow the teachings of Teene in combination with ordinary knowledge of a person having ordinary skill in the art to arrive at the invention specified in claim 4.

Regarding claim 5, Teene renders obvious the steps of modifying the first circuit description to generate the second circuit description with reduced parasitic information, wherein modifying comprises:

identifying circuit components marked as parasitic information; and

removing the parasitic information based on the identification.

It would have been obvious to a person of ordinary skill in the art to perform a method that follows Teene's method to produce a second circuit description with parasitic information included, and to remove that parasitic information to return to a previous stage in the method. This could result from a simulation involving the second circuit description including the parasitic information that reveals unacceptable performance or an error in the circuit design. It would then be common sense and common knowledge to a person of ordinary skill in the art to 1) optionally modify the second circuit design to address the problem, remove the parasitic information, and return to a previous step in the design process; or 2) remove the parasitic information, return to a previous step in the design process, and modify the design at a previous step to address the problem.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to follow the teachings of Teene in combination with ordinary knowledge of a person having ordinary skill in the art to arrive at the invention specified in claim 5.

Regarding claim 18, Teene discloses a simulator for simulating a circuit [*"More specifically, but without limitation thereto, the present invention relates to methods of*

representing an integrated circuit design for simulating the operation of the integrated circuit." (Teene, column 1, lines 8-12)], comprising:

means for reading a first description of the circuit that comprises a list of components in the circuit, the interconnections between the components, and parasitic information [*"FIG. 4 illustrates a flow diagram 400 for simulating a hierarchical integrated circuit design including only capacitance based on a logical netlist according to the prior art."* (Teene, column 3, lines 47-49)];

means for generating a second circuit description by removing at least a part of the parasitic information from the first circuit description [*"The functional simulation of FIG. 4 may include parasitic capacitance but generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation of the integrated circuit design."* (Teene, column 3, lines 60-64)]; and

means for simulating the circuit using substantially the first circuit description comprising the parasitic information and the second circuit description with reduced parasitic information [*"In the full instance resistance and capacitance extraction block 502, a layout extraction is performed to determine the values of all the parasitic capacitances and resistances in the integrated circuit design to generate the flat RC netlist for simulating the operation of the integrated circuit."* (Teene, column 4, lines 10-14)].

Teene's description involves generating a first circuit description without parasitic information, and subsequently generating parasitic information to combine with the first circuit description. Teene describes a similar method in FIGS. 14 and 15. Teene teaches that the method steps may be performed in another order [*"Although the method of the present invention*

illustrated by the flowchart descriptions above are described and shown with reference to specific steps performed in a specific order, these steps may be combined, sub-divided, or reordered without departing from the scope of the claims." (Teene, column 7, lines 44-48)].

It would have been obvious to a person of ordinary skill in the art to perform a method that follows Teene's method to produce a second circuit description with parasitic information included, and to remove that parasitic information to return to a previous stage in the method. This could result from a simulation involving the second circuit description including the parasitic information that reveals unacceptable performance or an error in the circuit design. It would then be common sense and common knowledge to a person of ordinary skill in the art to 1) optionally modify the second circuit design to address the problem, remove the parasitic information, and return to a previous step in the design process; or 2) remove the parasitic information, return to a previous step in the design process, and modify the design at a previous step to address the problem.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to follow the teachings of Teene in combination with ordinary knowledge of a person having ordinary skill in the art to arrive at the invention specified in claim 18.

18. Claims 6, 8, 9, 11, 13-16, and 19-23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Teene in view of US Pregrant Publication 2004/0083437 to Gullapalli et al. ("Gullapalli").

Regarding claim 6, Gullapalli teaches that simulating comprises solving a system of interrelated equations, wherein a part of the system of equations uses the first circuit description

and wherein a part of the system of equations uses the second circuit description [*"In block 14, circuit equations are generated based on the circuit description and models. These circuit equations embody the traditional circuit laws such as Kirchoff's voltage and current laws (KVL and KCL)... The result is a system of nonlinear differential equations that may be represented by: F(x) = b"* (Gullapalli, paragraph 0010).

Gullapalli and Teene are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gullapalli with Teene because Gullapalli expressly teaches a method that *"provide*[s] *for distortion analysis to measure the second and third order deviation of a circuit response from a desired linear response using only first order transfer functions."* (Gullapalli, paragraph 0008). Therefore, a person of ordinary skill would expect to achieve more accurate simulations by combining Gullapalli's teachings with Teene, and therefore to have higher confidence that the simulation accurately represents the performance of an analog device under design.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gullapalli and Teene to arrive at the invention specified in claim 6.

Regarding claim 8, Gullapalli teaches evaluating $F(X^i)$ using both the first and second simulation data structures for accuracy and performing a factorization of a Jacobian matrix built using only the first simulation data structure for increasing the speed of the simulation [*"As was described above, an iterative method can be applied to solve the nonlinear system of equations,*

F(x)=b. The iterative method can be described using the following iterative formula: [Equation 5] *In equation 5, J is the Jacobian matrix representing the first order transfer function of the system of equations a* x_0 *(analogous to* $(F'(x_0)$ *described above). That is, the first order transfer function of a system of equations can be represented as a Jacobian matrix. In equation 5, j is the number of the iteration. That is, for j=0 (corresponding to the first iteration), the first order response may be determined, as was described in reference to equation 2 above, where x was determined to be* x_1*, such that the resulting equation can be expressed as* $J(x_1)(x_1-x_0)=b-F(x_0)$*. Note that the approximation of x determined from equation 5 rapidly converges towards the actual solution of F(x)=b assuming that small signals are sufficiently small."* (Gullapalli, paragraphs 0021-0022)].

Regarding claim 9, Gullapalli teaches that simulating comprises solving a form of the equation $J\Delta X = -F(X^i)$ wherein J is a Jacobian matrix related to the circuit components, $F(X^i)$ is an evaluated equation, and ΔX is a variable to be solved, and further comprising factorizing the matrix J built using the second description, evaluating $F(X^i)$ using the first circuit description and solving for ΔX [*"As was described above, an iterative method can be applied to solve the nonlinear system of equations, F(x)=b. The iterative method can be described using the following iterative formula:* [Equation 5] *In equation 5, J is the Jacobian matrix representing the first order transfer function of the system of equations a* x_0 *(analogous to* $(F'(x_0)$ *described above). That is, the first order transfer function of a system of equations can be represented as a Jacobian matrix. In equation 5, j is the number of the iteration. That is, for j=0 (corresponding to the first iteration), the first order response may be determined, as was described in reference*

to equation 2 above, where x was determined to be x_1, such that the resulting equation can be expressed as $J(x_1)(x_1-x_0)=b-F(x_0)$. Note that the approximation of x determined from equation 5 rapidly converges towards the actual solution of F(x)=b assuming that small signals are sufficiently small." (Gullapalli, paragraphs 0021-0022)].

Regarding claim 11, Gullapalli teaches that simulating further comprises factorizing a Jacobian matrix built using the second circuit description for preconditioning a linear iterative solver (Gullapalli, paragraphs 0021-0022).

Regarding claim 13, Teene teaches an analog or RF simulator for simulating a circuit [*"More specifically, but without limitation thereto, the present invention relates to methods of representing an integrated circuit design for simulating the operation of the integrated circuit."* (Teene, column 1, lines 8-12)], comprising:

an elaboration engine that receives one or more lists associated with the circuit comprising a list of components in the circuit, interconnections between the components, and parasitic information and that defines two circuit descriptions, a first circuit description used for accuracy of the simulation and a second circuit description used for speed of the simulation, the first circuit description being different from the second circuit description [*"The functional simulation of FIG. 4 may include parasitic capacitance but generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation of the integrated circuit design."* (Teene, column 3, lines 60-64); *"In the full instance resistance and capacitance extraction block 502, a layout extraction is performed to determine the values*

of all the parasitic capacitances and resistances in the integrated circuit design to generate the flat RC netlist for simulating the operation of the integrated circuit." (Teene, column 4, lines 10-14)].

Gullapalli teaches a simulation kernel coupled to the elaboration engine that comprises at least a direct solver or linear iterative solver to simulate the circuit, wherein the simulation kernel solves a system of equations, part of the system of equations using the first circuit description and part of the system of equations using the second circuit description [*"As was described above, an iterative method can be applied to solve the nonlinear system of equations, F(x)=b. The iterative method can be described using the following iterative formula:* [Equation 5] *In equation 5, J is the Jacobian matrix representing the first order transfer function of the system of equations a* x_0 *(analogous to* $(F'(x_0)$ *described above). That is, the first order transfer function of a system of equations can be represented as a Jacobian matrix. In equation 5, j is the number of the iteration. That is, for j=0 (corresponding to the first iteration), the first order response may be determined, as was described in reference to equation 2 above, where x was determined to be* x_1*, such that the resulting equation can be expressed as* $J(x_1)(x_1-x_0)=b-F(x_0)$*. Note that the approximation of x determined from equation 5 rapidly converges towards the actual solution of F(x)=b assuming that small signals are sufficiently small."* (Gullapalli, paragraphs 0021-0022)]. Gullapalli and Teene are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gullapalli with Teene because Gullapalli expressly teaches a method that *"provide*[s] *for distortion analysis to measure the second and third order deviation of a circuit response from a desired linear response using only first order*

transfer functions." (Gullapalli, paragraph 0008). Therefore, a person of ordinary skill would expect to achieve more accurate simulations by combining Gullapalli's teachings with Teene, and therefore to have higher confidence that the simulation accurately represents the performance of an analog device under design.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gullapalli and Teene to arrive at the invention specified in claim 13.

Regarding claim 14, Gullapalli teaches a preconditioner coupled to the linear iterative solver (Gullapalli, paragraphs 0021-0022).

Regarding claim 15, Teene teaches that the one or more lists include a netlist and a DSPF comprising parasitic information [*"The functional simulation of FIG. 4 may include parasitic capacitance but generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation of the integrated circuit design."* (Teene, column 3, lines 60-64); *"In the full instance resistance and capacitance extraction block 502, a layout extraction is performed to determine the values of all the parasitic capacitances and resistances in the integrated circuit design to generate the flat RC netlist for simulating the operation of the integrated circuit."* (Teene, column 4, lines 10-14)].

Regarding claim 16, Gullapalli teaches that the simulation kernel evaluates $F(X^i)$ using the first circuit description and performs a factorization of a Jacobian matrix J using the second circuit description to solve an equation $J\Delta X = -F(X^i)$ (Gullapalli, paragraphs 0021-0022, et seq.).

Regarding claim 19, Gullapalli teaches means for solving a linear system of equations using an iterative solver or a direct solver (Gullapalli, paragraphs 0021-0022, et seq.).

Regarding claim 20, Gullapalli teaches that the means for simulating comprises evaluating $F(X^i)$ using the first circuit description and factorizing a Jacobian matrix J using the second circuit description to solve an equation $J\Delta X = -F(X^i)$ (Gullapalli, paragraphs 0021-0022, et seq.).

Regarding claim 21, Teene teaches a method of simulating a circuit using an analog or RF simulator [*"More specifically, but without limitation thereto, the present invention relates to methods of representing an integrated circuit design for simulating the operation of the integrated circuit."* (Teene, column 1, lines 8-12)], comprising:

defining two circuit descriptions to be used during the simulation, a first circuit description used for accuracy of the simulation and a second circuit description, different from the first circuit description, used for increasing the speed of the simulation; and simulating the circuit using both the first and second circuit descriptions [*"The functional simulation of FIG. 4 may include parasitic capacitance but generally does not include all the parasitic resistances, capacitances, and inductances that are required for accurate simulation of the integrated circuit*

design." (Teene, column 3, lines 60-64); *"In the full instance resistance and capacitance extraction block 502, a layout extraction is performed to determine the values of all the parasitic capacitances and resistances in the integrated circuit design to generate the flat RC netlist for simulating the operation of the integrated circuit."* (Teene, column 4, lines 10-14)].;

Gullapalli teaches generating a system of equations wherein a part of the system of equations uses a first circuit description comprising parasitic information and a part of the system of equations uses a second circuit description with parasitic information removed;

solving the system of equations in order to simulate the circuit; and

outputting the simulation results [*"As was described above, an iterative method can be applied to solve the nonlinear system of equations, F(x)=b. The iterative method can be described using the following iterative formula:* [Equation 5] *In equation 5, J is the Jacobian matrix representing the first order transfer function of the system of equations a* x_0 *(analogous to* $(F'(x_0)$ *described above). That is, the first order transfer function of a system of equations can be represented as a Jacobian matrix. In equation 5, j is the number of the iteration. That is, for* $j=0$ *(corresponding to the first iteration), the first order response may be determined, as was described in reference to equation 2 above, where x was determined to be* x_1*, such that the resulting equation can be expressed as* $J(x_1)(x_1-x_0)=b-F(x_0)$*. Note that the approximation of x determined from equation 5 rapidly converges towards the actual solution of* $F(x)=b$ *assuming that small signals are sufficiently small."* (Gullapalli, paragraphs 0021-0022)].

Gullapalli and Teene are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gullapalli with Teene because Gullapalli

expressly teaches a method that *"provide*[s] *for distortion analysis to measure the second and third order deviation of a circuit response from a desired linear response using only first order transfer functions."* (Gullapalli, paragraph 0008). Therefore, a person of ordinary skill would expect to achieve more accurate simulations by combining Gullapalli's teachings with Teene, and therefore to have higher confidence that the simulation accurately represents the performance of an analog device under design.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of Gullapalli and Teene to arrive at the invention specified in claim 6.

Regarding claim 22, Gullapalli teaches that generating the system of equations comprises solving a form of the equation $J\Delta X = -F(X^i)$ wherein J is a Jacobian matrix related to the circuit components, $F(X^i)$ is an evaluated solution, and ΔX is a variable to be solved (Gullapalli, paragraphs 0021-0022, et seq.).

Regarding claim 23, Gullapalli teaches that solving further comprises factorizing the Jacobian matrix J built using the modified circuit description, evaluating $F(X^i)$ using the first circuit description, and solving for ΔX (Gullapalli, paragraphs 0021-0022, et seq.).

19. Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Teene in view of US Patent No. 6,530,065 to McDonald et al. ("McDonald").

Regarding claim 12, McDonald teaches receiving, on a server computer, a circuit description from a client computer over a distributed network, simulating the description on the server computer, and returning simulation results to the client computer over the distributed network [*"Referring to FIG. 1A, an example of software architecture employed by a server for providing simulation tools is shown as a system 100."* (McDonald, column 5, line 17 et seq.); "*When generating the stored netlists, a developer may employ a block level editor or schematic editor 114 to create such netlists. Examples of schematic editors include Concept from Cadence Design Systems, and Rapid Circuit Development Tool ("RCD") from Transim Technology corporation, as well as others known to those skilled in the relevant art."* (McDonald, column 5, lines 60-66)]; *"Under the server system 100, the server initiates a simulation. Using SIMPLIS (which may be forty times faster than PSPICE), waveform simulations are typically completed within two minutes under the simulation control block. Waveform data is then processed under the waveform processing block and downloaded to the user's web browser 101 to be displayed and further processed using a Java-based waveform viewer, described below."* (McDonald, column 6, lines 42-55)].

Teene and McDonald are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of McDonald and Teene as expressly motivated by Teene to provide an online design center that allows end users to quickly select, try and evaluate the manufacturer's products (McDonald, column 4, lines 39-57). Therefore, the combination would enhance the usability of the circuit simulator taught by Teene.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of McDonald and Teene to arrive at the invention specified in claim 12.

20. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Teene in view of Gullapalli as applied to claim13 above, and further in view of McDonald.

Regarding claim 17, McDonald teaches a network coupled to the simulator through which the first circuit description is received (McDonald, FIG. 1A, "Internet").

Teene in view of Gullapalli and McDonald are analogous art because both are drawn to circuit simulation.

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of McDonald and Teene in view of Gullapalli as expressly motivated by Teene to provide an online design center that allows end users to quickly select, try and evaluate the manufacturer's products (McDonald, column 4, lines 39-57). Therefore, the combination would enhance the usability of the circuit simulator taught by Teene.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the teachings of McDonald and Teene in view of Gullapalli to arrive at the invention specified in claim 17.

Conclusion

Art considered relevant by the Examiner has been cited on form PTO-892.

Kenneth S. Kundert et al., "Achieving Accurate Results with a Circuit Simulator" teaches an iterative method for simulating a circuit (Kundert, § 2.1 Isolated Solution). Kundert expressly teaches removing parasitic components from a circuit description in order to accelerate the circuit simulation with no loss of accuracy or a negligible loss of accuracy (Kundert, § 3.1 Model Accuracy).

Geoff Dawe, "Design and Simulation of an RF Transceiver ASIC", teaches a method of simulating analog RF circuits (Dawe, page 2). Dawe's method includes simulating the design without parasitic information included, and simulating the design with parasitic information included (See, for example, Dawe, page 22, Figure 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez can be reached at (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR)

system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jason Proctor/
Primary Examiner
Art Unit 2123

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